A V-band Power Amplifier in 0.13-um CMOS (Invited paper)
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Introduction

The 60-GHz wireless personal area network (WPAN) is an attractive application for next-generation high-speed wireless network. Two types of 60-GHz radios are considered, the first one is the one-way radio for video streaming or download applications and the second one is the two-way radio for multi-gigabit files transfer. CMOS technology is advantaged to develop the 60-GHz front-end building blockings because of its maturity, low cost and high-level integration. Power amplifier is the most challenging circuit of the CMOS millimeter-wave front-end building blocks due to the low breakdown voltage of the CMOS transistors and high loss of the passive elements. Recently, a numbers of V-band power amplifiers were reported using 90-nm CMOS technologies, and the highest saturated power is 12.3 dBm [1]-[5].

In this paper, a V-band CMOS power amplifier fabricated using 0.13-μm CMOS process is presented with a maximum output power of 14.3 dBm and a $P_{1\text{dB}}$ of 11.2 dBm at 55 GHz. The linear gain is 15.5 dB, and the maximum PAE is 8%.

Circuit Design

The V-band power amplifier was implemented in 0.13-μm 1P8M CMOS which has a $f_T$ of 91 GHz and a $f_{\text{max}}$ of 108 GHz. This process provides 3.4-μm thickness top metal for low-loss interconnections and metal-insulator-metal (MIM) capacitor of 1 fF/μm².

In this power amplifier design, the cascode device configuration is selected to achieve high gain performance. Figure 1 shows the schematic of the V-band power amplifier which is a 3-stage single-ended design. For the second and third stages, the common-source and common-gate devices are both selected to be 32 fingers with 3-μm unit finger width. The 72-μm width transistors are selected for the first stage to obtain a better power added efficiency. The matching networks are implemented by using the thin-film microstrip line (TFMS) consists of top metal (M8) as signal line and bottom metal (M1) as ground plane. The output of the third stage is matched for maximum output power and the inter-stage and input matching network are designed for gain and input return loss. All the matching networks, including the MIM capacitors, pad parasitic capacitance, and TFMS lines were simulated using full-wave EM simulator (Sonnet 11.52) [6]. The complete circuit was then simulated using ADS [7]. Figure 2 shows the chip photo, and the chip size is 0.66 mm x 0.5 mm.

Measurements

This V-band power amplifier was measured via on-wafer probing. All of the transistors are biased at class-A condition. The drain voltage is 3 V, and the currents of the first, second and third stage are 10, 42 and 42 mA, respectively. The measured small-signal gain and return losses are shown in Figure 3. This
amplifier demonstrates a peak gain of 15.5 dB at 55 GHz, and the 3-dB bandwidth is from 47 to 61 GHz. The output power and PAE versus input power at 55 GHz are shown in Figure 4, a 14.3-dBm saturated power and an 11.2-dBm $P_{1dB}$ are obtained. The maximum measured PAE of this power amplifier is 8 %.

Table I summarizes the recently reported V-band CMOS power amplifiers. The previously reported V-band CMOS power amplifiers were fabricated by 90-nm technologies, and the highest saturation power is 12.3 dBm. Our V-band power amplifier using 0.13-μm CMOS technology has a 14.3-dBm saturated power and 15.5-dB linear gain and demonstrates the best PA performance in 0.13-μm CMOS at V-band.

**Conclusion**

The highest output power V-band PA using 0.13-μm CMOS process has been successfully developed. This power amplifier demonstrates high gain, PAE, and output power with a small chip size.

**References**


Figures

Figure 1. Schematic of the V-band CMOS power amplifier.

Figure 2. Chip photo of the V-band CMOS power amplifier.
Figure 3. Measured small-signal gain and return losses.

Figure 4. Measured output power and PAE versus input power.

Table I. Comparison of the recently reported V-band CMOS power amplifiers.

<table>
<thead>
<tr>
<th>Reference</th>
<th>Process</th>
<th>Center freq. (GHz)</th>
<th>Gain (dB)</th>
<th>OP_{1dB} (dBm)</th>
<th>P_{sat} (dBm)</th>
<th>PAE (%)</th>
<th>Chip size (mm²)</th>
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<tr>
<td>This work</td>
<td>130-nm CMOS</td>
<td>55</td>
<td>15.5</td>
<td>11.2</td>
<td>14.3</td>
<td>8</td>
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<td>[1]</td>
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<td>5.2</td>
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<td>3.1</td>
<td>8.2</td>
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<td>-</td>
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<tr>
<td>[4]</td>
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<td>8.5</td>
<td>4.7</td>
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<tr>
<td>[5]</td>
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<td>15.6</td>
<td>10.5</td>
<td>11.5</td>
<td>8.2</td>
<td>-</td>
</tr>
</tbody>
</table>

[1] 90-nm CMOS
[2] 90-nm CMOS
[3] 90-nm CMOS
[4] 90-nm CMOS
[5] 90-nm CMOS